ISSN 2349-7815

International Journal of Recent Research in Electrical and Electronics Engineering (IJRREEE)
Vol. 3, Issue 3, pp: (23-30), Month: July - September 2016, Available at: www.paperpublications.org

Harmonic Distortion Analysis of Output Voltage in Multilevel Cascaded H-bridge Multilevel Inverter for RL Load

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Abstract: **Multilevel inverter output voltage produce a staircase output waveform, this waveform look like a sinusoidal waveform. The multilevel output voltage having less number of harmonics compare to conventional bipolar inverter output voltage. The desired output of a multilevel inverter is synthesized by several sources of DC voltage. With an increasing number of DC voltage sources, the converter output voltage waveform approaches nearly sinusoidal waveform while using a fundamental switching frequency scheme.**

Based on the topology multilevel inverters are classified as: (i) Diode-clamped multi-level inverter (ii) Flying-capacitor multi-level inverter (iii) Cascaded H-bridge multi level inverter

While each of these converters fulfils the basic requirements of a multilevel inverter advantages, there are also some disadvantages associated with them.

(i) A diode clamped inverter uses many clamping diodes with the increase in level in output voltage. The diode reverse voltage rating differs for each level and has to be calculated each time as the number of level increases.

(ii) In flying capacitor inverter, the number of storage capacitors required increases with increase in levels. Balancing the charging and discharging rates of the capacitor is also a problem.

(iii) In cascaded H-bridge inverter which requires reduced number of electronic devices as compared to other two topologies, there is a drawback of increased number of sources with increase in the output voltage.

In this paper Harmonic distortion analysis of output voltage in a cascaded H-bridge multilevel inverter at different conduction angles is presented with the help of simulink / matlab.

Keywords: **Harmonic distortion, multilevel inverter, conduction angle, harmonic factor, Cascaded H-bridge inverter.**

I. INTRODUCTION

The cascaded H-bridge inverter has drawn tremendous interest due to the great demand of medium-voltage high-power inverters. It is composed of multiple units of single-phase H-bridge power cells. The H-bridge cells are normally connected in cascade on their ac side to achieve medium voltage operation and low harmonic distortion. The cascade H-bridge multilevel inverter requires a number of isolated dc supplies, each of which feeds a H-bridge power cell.

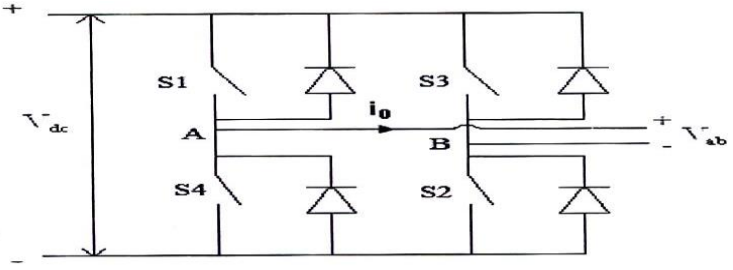

Fig. 1 Single phase 3-level H-bridge inverter

The steps to synthesize the staircase output voltage are as follows:

- The single phase H-bridge cell shown in fig 1, which is the building block for the cascaded H-bridge inverter is associated with separate dc sources.
- The inverter dc bus voltage V_{dc} is usually fixed, while its ac output voltage V_{ac} can be adjusted by either bipolar or unipolar modulation schemes. With different combinations of four switches, S1 to S4, each inverter level can generate three different voltages at the output $+V_{dc}$, $-V_{dc}$ and 0.
- During inverter operation, switch S1 and S2 are closed at the same time to provide V_{dc} a positive value and a current path for I_o. Switch S3 and S4 are turned on to provide V_{dc} a negative value with a path for I_o. Depending on load current angle, the current may flow through the main switch or freewheeling diodes are connected anti parallel with each switch.

In case of zero level, there are two possible switching patterns to synthesize zero level, they are:

(a) S1 and S3 on, S2 and S4 off

(b) S1 and S3 off and S2 & S4 on.

A simple gate signal, repeated zero level patterns is shown in fig 2.

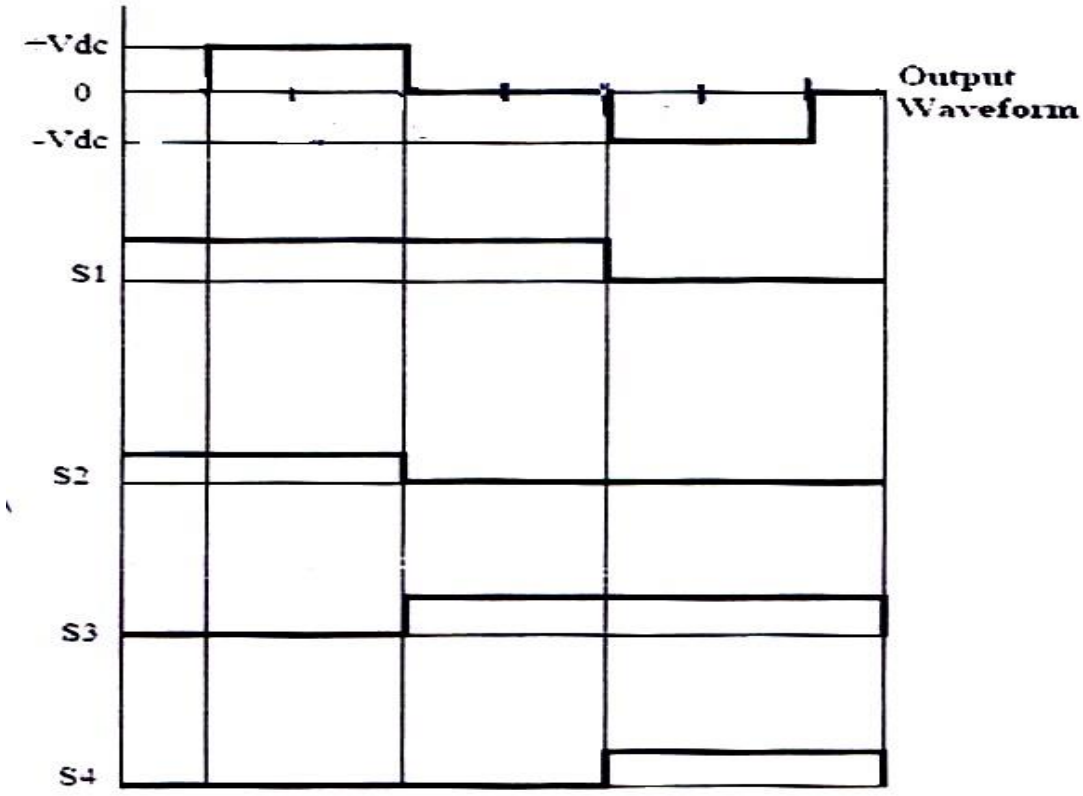

Fig.2 Repeated Zero-level switching pattern

All zero levels are generated by turning on S1 and S3. Level 1 represents the state when the gate is turned on, and level 0 represents the state when the gate is turned off. S1 & S3 are turned on longer than S2 & S4 in each cycle because the same zero level switching patterns are used. As a result, S1 and S3 consume more power, getting higher temperature than the other two switches. To avoid this problem, a different switching pattern for zero level is applied.
In the first zero stage S1 and S3 are turned on, then in the second zero stage, S2 and S4 are turned on instead of S1 and S3. By applying this method, turn-on time for each switch turns out to be equal as shown in fig 3. It is known as swapped zero-level switching pattern.

ISSN 2349-7815

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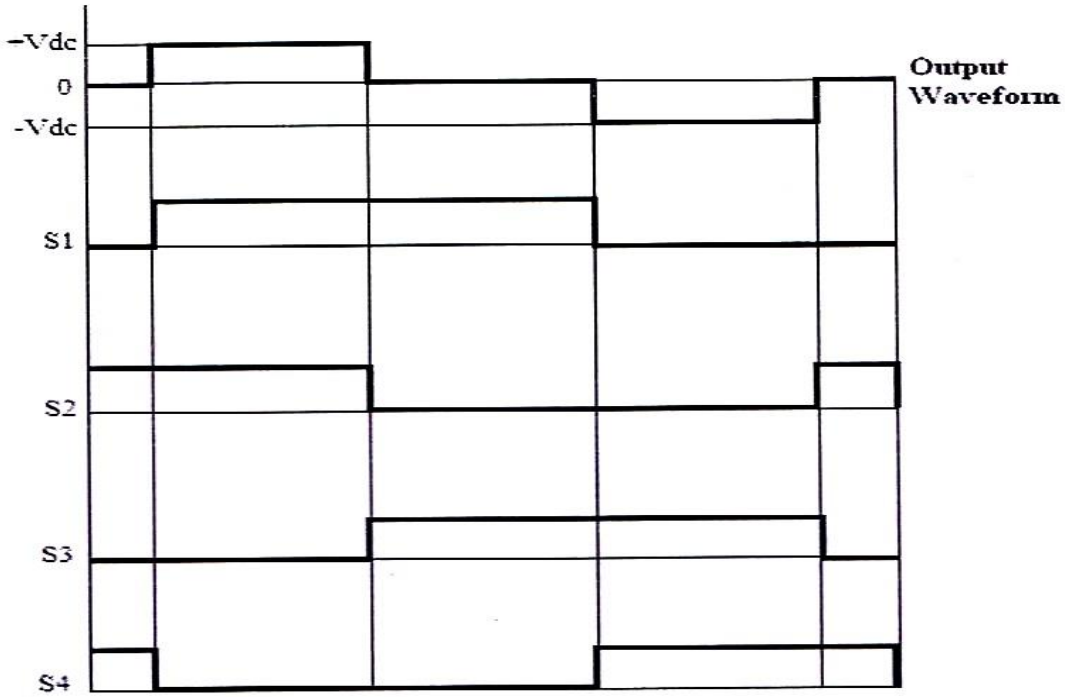

Fig . 3 Swapped zero-level switching pattern

II. SIMULINK MODEL

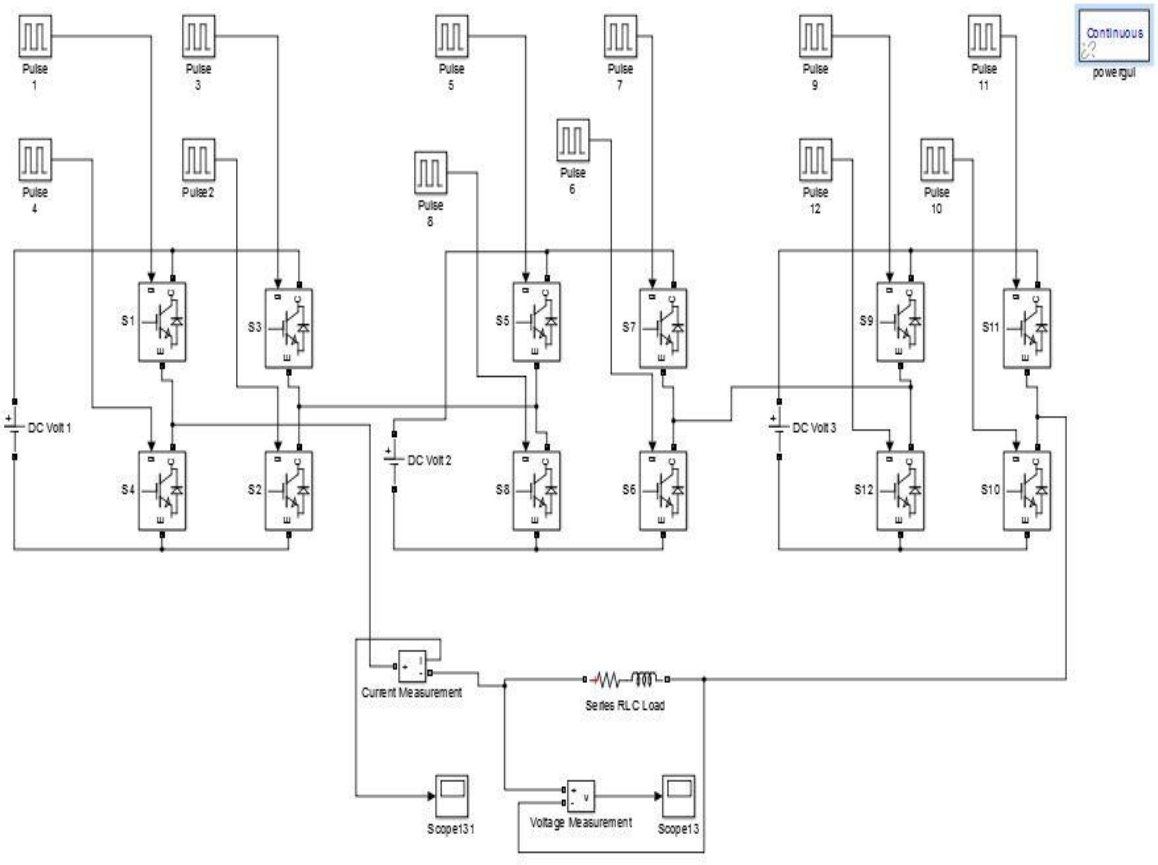

Fig 4. Simulink model of 7-level inverter

ISSN 2349-7815

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III. RESULTS

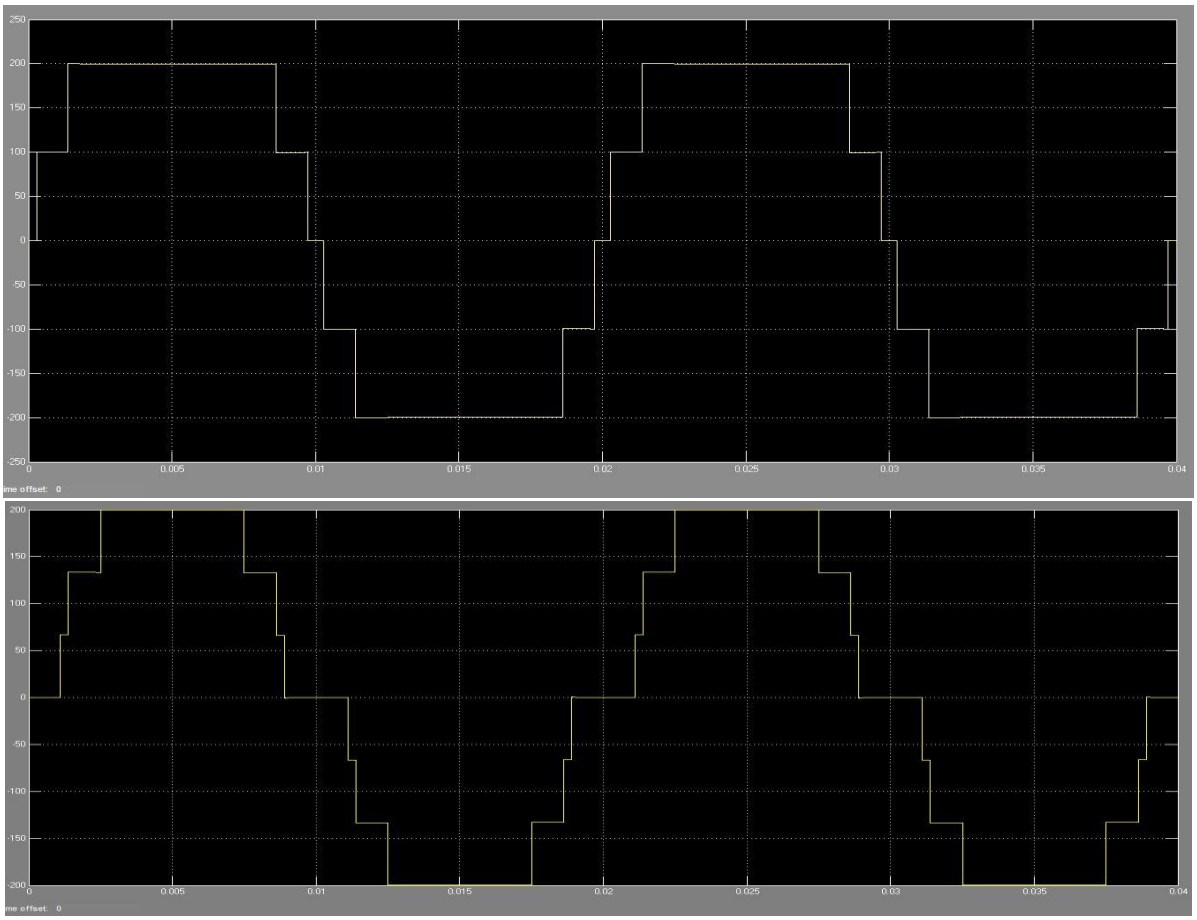

Fig. 5 Output voltage of 5 and 7 level inverters

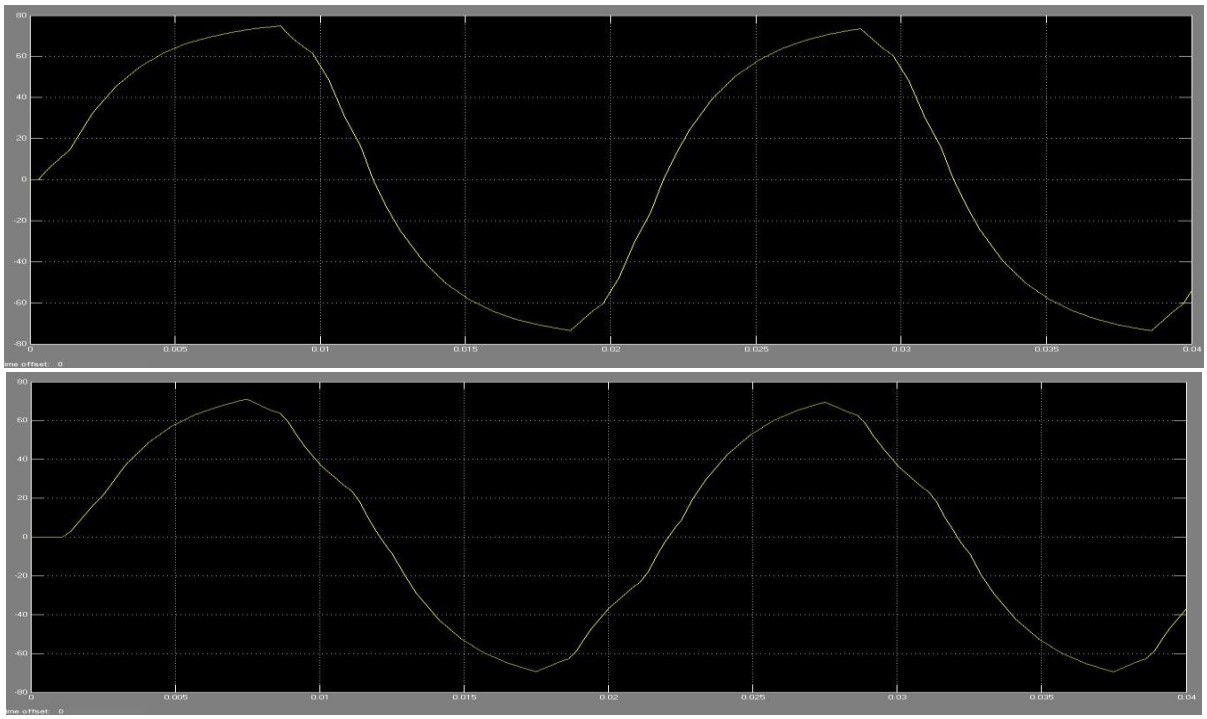

Fig. 6 Load current of 5 and 7 level inverters

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Table 1. Total Harmonic distortion (THD) of output voltage and Current in a 5-level cascaded H-bridge inverter at different combinations of conduction angles

Conduction Angles	$\varphi_1 = 90^0$		$\varphi_1 = 120^0$		$\varphi_1 = 130^0$	
	$\%V_{THD}$	$\%I_{THD}$	$\%V_{THD}$	$\%I_{THD}$	$\%V_{THD}$	$\%I_{THD}$
$\varphi_2 = 120^0$	28.93	15.7	_	_	_	_
$\varphi_2 = 130^0$	23.15	14.44	26.25	14.68	_	_
$\varphi_2 = 140^0$	17.8	14.88	23.54	16.4	26.55	16.21
$\varphi_2 = 150^0$	17.29	13.89	20.34	15.82	23.79	17.07
$\varphi_2 = 160^0$	17.16	15.9	21.19	18	22.94	18.35
$\varphi_2 = 170^0$	19.65	17	24	17.99	24	19.35
nduction angles	$\varphi_1 = 140^0$		$\varphi_1 = 150^0$		$\varphi_1 = 160^0$	
	$\%V_{THD}$	$\%I_{THD}$	$\%V_{THD}$	$\%I_{THD}$	$\%V_{THD}$	$\%I_{THD}$
$\varphi_2 = 150^0$	27	19.29	_	_	_	_
$\varphi_2 = 160^0$	27.05	19.78	28.51	22.2	_	_
$\varphi_2 = 170^0$	29.97	21.86	25.16	23.35	28.5	22.02

Table 2. Total Harmonic distortion (THD) of output voltage and current in a 7-level cascaded H-bridge inverter at different combinations of conduction angles

Conduction angles	$\varphi_1 = 90^0$ $\varphi_2 = 120^0$		$\varphi_1 = 120^0$ $\varphi_2 = 130^0$		$\varphi_1 = 130^0$ $\varphi_2 = 140^0$	
	$\%V_{THD}$	$\%I_{THD}$	$\%V_{THD}$	$\%I_{THD}$	$\%V_{THD}$	$\%I_{THD}$
$\varphi_2 = 130^0$	22.34	14.57	_	_	_	_
$\varphi_2 = 140^0$	18.5	14.59	23.68	15.14	_	_
$\varphi_2 = 150^0$	13.13	14.55	20.36	15.58	24	17.24
$\varphi_2 = 160^0$	12.91	13.97	18.19	16.79	22.8	17.46
$\varphi_2 = 170^0$	13.3	16.74	20.13	17.83	21.56	19.53

Conduction angles	$\varphi_1 = 140^0$ $\varphi_2 = 150^0$		$\varphi_1 = 150^0$ $\varphi_2 = 160^0$	
	$\%V_{THD}$	$\%I_{THD}$	$\%V_{THD}$	$\%I_{THD}$
$\varphi_2 = 150^0$	24	17.24	_	_
$\varphi_2 = 160^0$	22.8	17.46	27.75	20.52
$\varphi_2 = 170^0$	21.56	19.53	27.16	21.44

Table 3. Output voltage THD and harmonic factor at different combinations of conduction angle (φ_1, φ_2 , φ_3) in a 7-level cascaded H-bridge inverter

Order of harmonic	$\varphi_1 = 90^0$ $\varphi_2 = 110^0$ $\varphi_3 = 170^0$ V_{THD} = 15.94 %	$\varphi_1 = 90^0$ $\varphi_2 = 120^0$ $\varphi_3 = 160^0$ V_{THD} = 12.91 %	$\varphi_1 = 90^0$ $\varphi_2 = 120^0$ $\varphi_3 = 170^0$ V_{THD} =13.3 %
DC	.01 %	0.66 %	0. 97 %
2nd	.02 %	1.26 %	1.48 %
3rd	1.66 %	1.62 %	4.1 %
4th	.01 %	1.05 %	0.29 %
5th	6.54 %	7.84 %	4.75 %
6th	0.01 %	0.7 %	1.04 %

7th	6.54 %	0.84 %	3.59 %
8th	0 %	0.27 %	1.87 %
9th	9.44 %	2.84 %	5.64 %
10th	0 %	0.18 %	1.8 %
11th	2.8 %	1.14 %	2.6 %
12th	0 %	0.62 %	0.87 %
13th	2.62 %	1.99 %	2.63 %

Order of harmonic	$\varphi_1 = 90^0$ $\varphi_2 = 130^0$ $\varphi_3 = 170^0$ V_{THD} = 12.21 %	$\varphi_1 = 90^0$ $\varphi_2 = 140^0$ $\varphi_3 = 170^0$ V_{THD} = 13.81 %	$\varphi_1 = 90^0$ $\varphi_2 = 130^0$ $\varphi_3 = 140^0$ V_{THD} = 17.1 %
DC	1.05 %	0.45 %	0. 01 %
2nd	2.07 %	1.79 %	0.01 %
3rd	5.94 %	8.84 %	1.55 %
4th	0.75 %	1.16 %	0.01 %
5th	3.11 %	0.4 %	11.41 %
6th	1.09 %	0.55 %	0.01 %
7th	2.76 %	4.2 %	6.29 %
8th	0.32 %	0.72 %	0.00 %
9th	2.11 %	1.93 %	4.84 %
10th	1.15 %	1 %	0.00 %
11th	1.32 %	3.23 %	4.92 %
12th	0.85 %	1.16 %	0.0 %
13th	1.51 %	0.92 %	1.37 %

Table 4. Minimum Output voltage THD and harmonic factor at different combinations of conduction angle (φ_1, φ_2 , φ_3) in a 7-level cascaded H-bridge inverter

Order of harmonic	$\varphi_1 = 90^0$ $\varphi_2 = 120^0$ $\varphi_3 = 150^0$ V_{THD} = 13.13 %	$\varphi_1 = 90^0$ $\varphi_2 = 120^0$ $\varphi_3 = 160^0$ V_{THD} = 12.91 %	$\varphi_1 = 90^0$ $\varphi_2 = 130^0$ $\varphi_3 = 170^0$ V_{THD} = 12.21 %
DC	.01 %	0.66 %	1.05 %
2nd	.01 %	1.26 %	2.07 %
3rd	0.01 %	1.62 %	5.94 %
4th	.01 %	1.05 %	0.75 %
5th	8.9 %	7.84 %	3.11 %
6th	0.01 %	0.7 %	1.09 %
7th	0.85 %	0.84 %	2.76 %
8th	0 %	0.27 %	0.32 %
9th	0.0 %	2.84 %	2.11 %
10th	0.0 %	0.18 %	1.15 %
11th	3.27 %	1.14 %	1.32 %
12th	0 .0 %	0.62 %	0.85 %
13th	1.92 %	1.99 %	1.51 %

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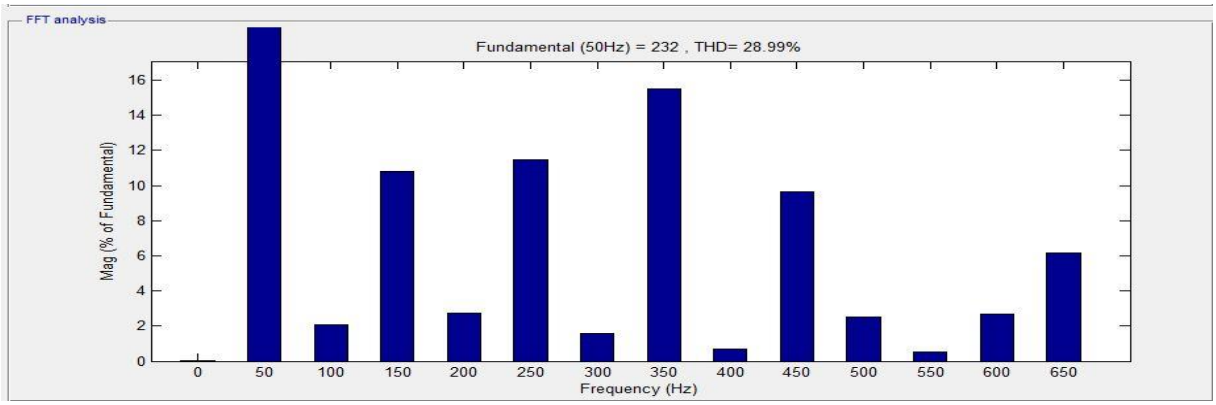
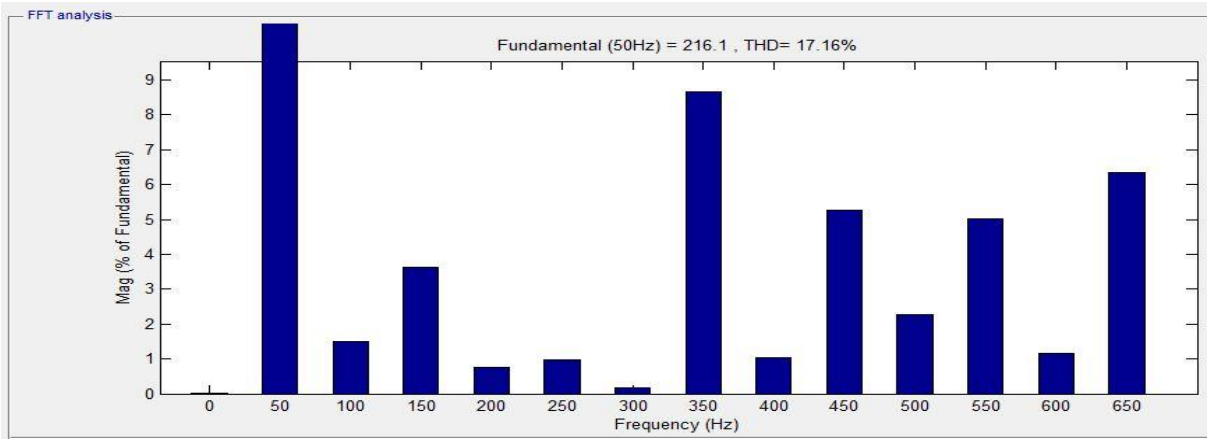


(a)



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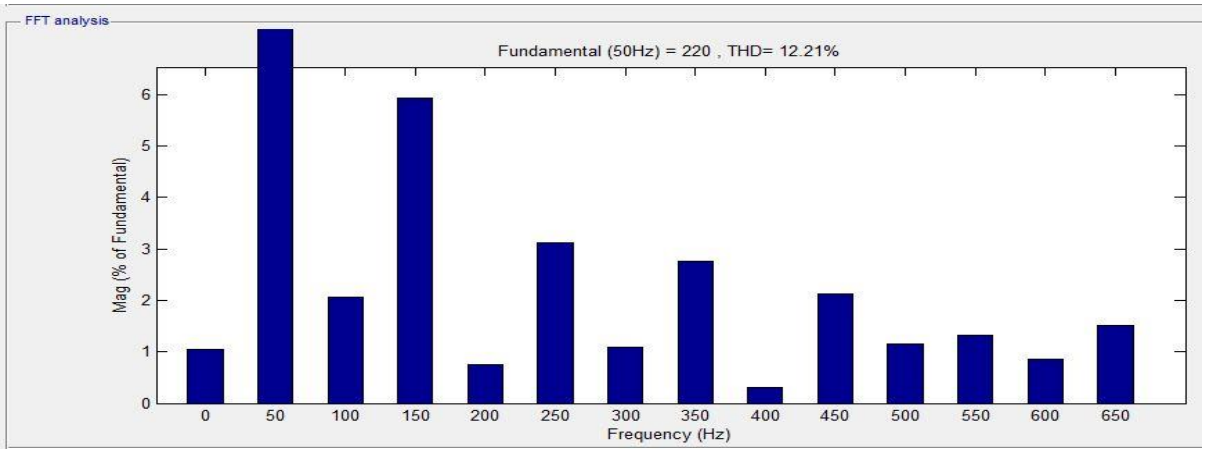

(c)

Fig. 7 .Harmonic spectra of minimum voltage THD (a)3-level inverter (b) 5-level inverter (c) 7-level inverter

IV. CONCLUSIONS

- Table1 and 2 shows total harmonic distortion (THD) of the output voltage and current in 5 & 7 level inverters for different conduction angles.
- From fig.6 it is clear that load current of 7-level inverter is closer to the sinusoidal shape as compare to current in 5-level inverter.

- From table 3 it is clear that for some combinations of conduction angles, the harmonic factor of some lower order harmonics is very negligible or almost nearer to zero.
- Fig 7 shows the harmonic spectra of output voltage in 3, 5 and 7 level inverter.

REFERENCES

[1] Muhammad H. Rashid, Third edition, "Power electronics circuits, devices and applications", Practice Hall of India.

[2] Jainil K. Shah, Manish S. Patel, "Comparative analysis of single phase cascaded H-bridge multilevel inverter", IJIREEICE, ISSN: 2321-2004,Vol. 3, Issue April 2015.

[3] Nitin Tyagi , Bharti Yadav , "Performance analysis of 5-level H-bridge multilevel inverter", IJTRE, ISSN 2347-4718,Vol. 2, Issue 9, May-2015